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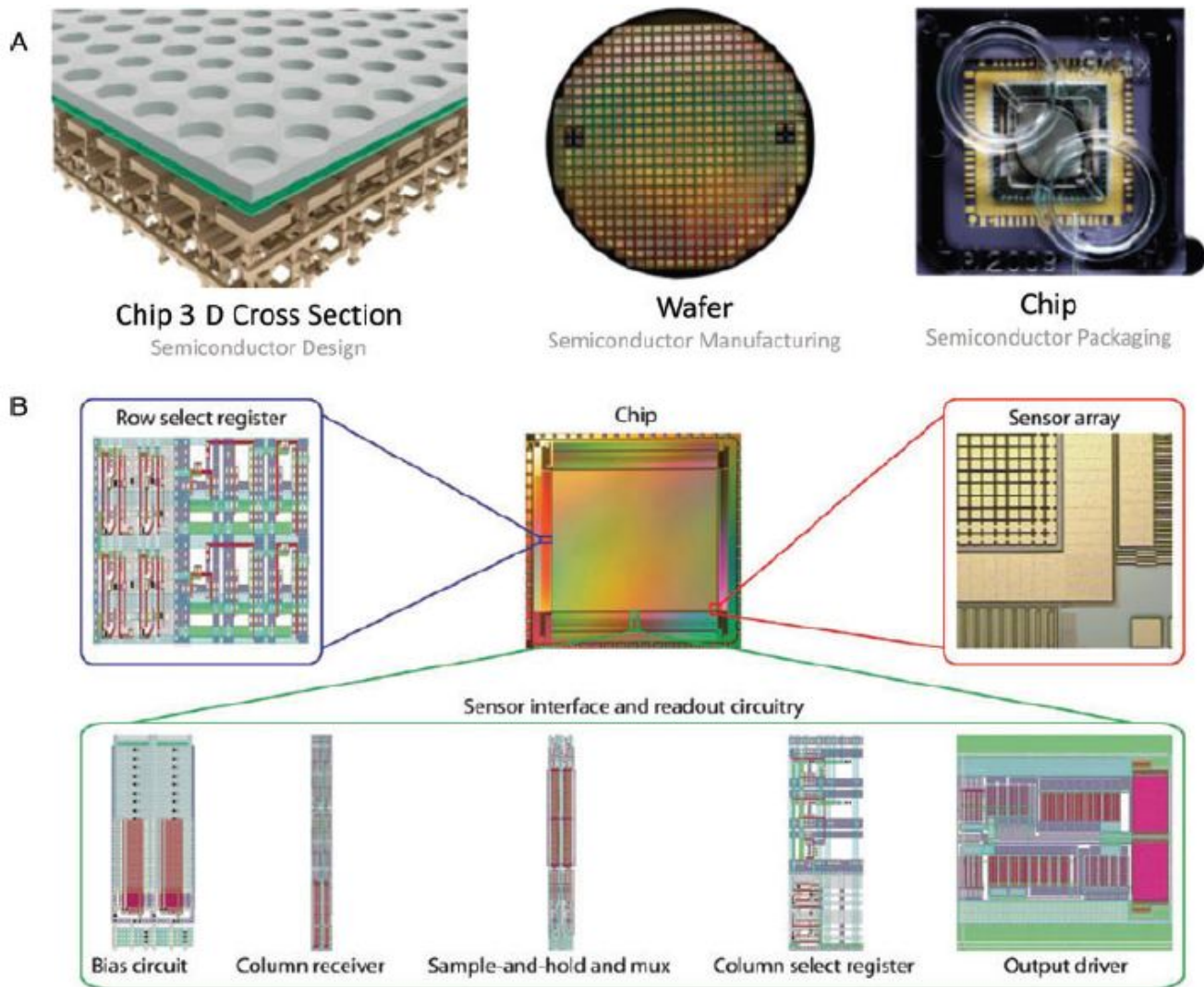


Figure 3. Major elements of chip design, fabrication and architecture. (A) Chips are designed using standard CMOS design tools. Fabrication is done at the wafer level in standard CMOS fabs. The chips are diced and packaged, including the outer flow cell, using standard chip packaging processes, resulting in the chip shown, an Ion Torrent 314 chip. (B) The major functional blocks of the ion chip are shown: Chip, with row select registers, to sequentially address each row, and sensor array, showing close up of the individual metal floating plates, Sensor interface and readout circuitry, containing bias circuits, to set the operating current, column receiver to set the operating voltage, sample-and-hold and mux, to capture the output voltage, column select register to sequentially address each column, and output driver to transmit voltages off-chip for external data acquisition.

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